Please amend the application as follows:

AMENDMENTS TO THE CLAIMS:

Please cancel claim 48 without disclaimer or prejudice.

1. (Original) A data processing system comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to the bus;

(c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising:

a virtual memory addressing unit;

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path; and

a multi-precision execution unit coupled to the data path, the multi-precision execution unit configurable to dynamically partition data received from the data path to account for an elemental width of the data wherein the elemental width of the data is equal to or narrower than the data path, the multi-precision execution unit being capable of performing group floating-point operations on multiple operands in partitioned fields of operand registers and returning catenated results.

2. (Original) The data processing system of claim 1 wherein the multi-precision execution unit is capable of performing group add, group subtract and group multiply arithmetic operations on catenated floating-point data and, for each such group operation, returning catenated results of the operation to a register.

3. (Original) The data processing system of claim 1 wherein at least some of the group add, group subtract and group multiply arithmetic operations perform arithmetic operations on floating-point data stored in first and second operand registers and return the catenated result to a result register.

4. (Original) The data processing system of claim 3 wherein the result register is a different register than either the first or second operand registers.

5. (Original) The data processing system of claim 1 wherein the multi-precision execution unit is capable of executing a first plurality of group floating-point operations on floating-point data of a first precision and a second plurality of group floating-point operations on floating-paint data of a second precision that is a higher precision than the first precision and wherein a number of data elements stored in partitioned fields of the operand registers for the first and second plurality of group floating-point operations is inversely related to the precision of the data elements.

6. (Original) The data processing system of claim 1 wherein the multi-precision execution unit is capable of executing group floating point operations that operate on 32-bit data elements and group floating-paint operations that operate an 64-bit data elements and wherein a number of data elements stored in partitioned fields of operand registers used for the operations that operate on 32-bit data elements is twice as many as a number of data elements stored in

partitioned fields of operand registers used for the operations that operate on 64-bit data elements.

7. (Original) The data processing system of claim 1 wherein, when performing at least some of the group floating-point operations, the multi-precision execution unit operates on partitioned fields of operand registers in parallel and returns the catenated results to a register.

8. (Original) The data processing system of claim 1 wherein the multi-precision execution unit is capable of executing a plurality of group floating-point operations on floating-point data of a first precision and a plurality of group floating-point operations on floating-point data of a second precision that is a higher precision than the first precision and wherein, when performing at least one of the group floating-point operations on floating-point data of the first precision, the multi-precision execution unit operates on at least two partitioned operands in parallel.

9. (Original) The data processing system of claim 1 wherein the multi-precision execution unit is capable of performing group floating-point operations on catenated data having a total aggregate width of 128 bits.

10. (Original) The data processing system of claim 1 wherein the multi-precision execution unit is capable of performing group floating-point operations on floating-point data of more than one precision.

11. (Original) The data processing system of claim 1 wherein the multi-precision execution unit is capable of performing group integer operations on multiple operands in partitioned fields of operand registers and returning catenated results to a register.

12. (Original) The data processing system of claim 11 wherein the multi-precision execution unit is capable of performing group add, group subtract and group multiply arithmetic operations on catenated integer data and, for each such group operation, returning catenated results of the operation to a register.

13. (Original) The data processing system of claim 12 wherein at least some of the group add, group subtract and group multiply arithmetic operations perform arithmetic operations on integer data stored in first and second operand registers and return the catenated result to a result register.

14. (Original) The data processing system of claim 11 wherein the multi-precision execution unit is capable of executing a first plurality of group integer operations on integer data of a first precision and a second plurality of group integer operations on integer data of a second precision that is a higher precision than the first precision and wherein a number of data elements stored in partitioned fields of the operand registers for the first and second plurality of group integer operations is inversely related to the precision of the data elements.

15. (Original) The data processing system of claim 11 wherein, when performing at least some of the group integer operations, the multi-precision execution unit operates on partitioned fields of operand registers in parallel and returns the catenated results to a register.

16. (Original) The data processing system of claim 11 wherein the multi-precision execution unit is capable of executing a plurality of group integer operations on integer data of a first precision and a plurality of group integer operations on integer data of a second precision that is a higher precision than the first precision and wherein, when performing at least one of the

group integer operations on integer data of the first precision, the multi-precision execution unit operates on at least two partitioned operands in parallel.

17. (Original) The data processing system of claim 1 wherein the multi-precision execution unit is capable of performing one or more group data handling operations that operate on multiple operands in partitioned fields of one or more operand registers and returning catenated results to a register.

18. (Original) The data processing system of claim 17 wherein the one or more group data handling operations comprises a first group operation that converts a plurality of n-bit data elements in a first operand register and a plurality of n-bit data elements in a second operand register into a plurality of n/2-bit data elements in a result register.

19. (Original) The data processing system of claim 18 wherein the first group operation shifts each of the plurality of n/2-bit data elements by a specified number of bits during the conversion.

20. (Original) The data processing system of claim 17 wherein the one or more group data handling operations comprises a second group operation that interleaves a plurality of data elements selected from a first operand register with a plurality of data elements selected from a second operand register and catenates the data elements into a result register.

21. (Original) The data processing system of claim 17 wherein the one or more data handling operations comprises a group shift left operation that shifts bits of individual data elements catenated in an operand register to the left and clears empty low order bits of the individual data elements to zero.

22. (Original) The data processing system of claim 17 wherein the one or more data handling operations comprises a group shift right operation that shifts bits of individual data elements catenated in an operand register to the right and fills empty high order bits of the individual data elements with a value equal to a value stored in a sign bit of the individual data element.

23. (Original) The data processing system of claim 17 wherein the one or more data handling operations comprises a group shift right operation that shifts bits of individual data elements catenated in an operand register to the right and clears empty high order bits of the individual data elements to zero.

24. (Original) The data processing system of claim 17 wherein the multi-precision execution unit is capable of executing a first plurality of group data handling operations on data of a first precision and a second plurality of group data handling operations on data of a second precision that is a higher precision than the first precision and wherein a number of data elements stored in partitioned fields of the operand registers for the first and second plurality of group data handling operations is inversely related to the precision of the data elements.

25. (Original) The data processing system of claim 17 wherein, when performing at least some of the group data handling operations, the multi-precision execution unit operates on partitioned fields of operand registers in parallel and returns the catenated results to a register.

26. (Original) The data processing system of claim 17 wherein the multi-precision execution unit is capable of executing a plurality of group data handling operations on data of a first precision and a plurality of data handling operations on data of a second precision that is a higher precision than the first precision and wherein, when performing at least one of the group

data handling operations on data of the first precision, the multi-precision execution unit operates on at least two partitioned operands in parallel.

27. (Original) The data processing system of claim 1 wherein the multi-precision execution unit comprises a plurality of functional units.

28. (Original) The data processing system of claim 1 wherein the at least one register file comprises a plurality of registers that can be used to store operands and results for the group floating-point operations.

29. (Original) The data processing system of claim 1 wherein the multi-precision execution unit returns the catenated results to a register.

30. (Original) The data processing system of claim 1 wherein the at least one register file comprises a plurality of general purpose registers that can be used as operand and result registers for group floating-point operations.

31. (Previously Presented) The system of claim 1, wherein the operand registers are within the at least one register file.

32. (Previously Presented) The data processing system of claim 1, wherein the multi-precision execution unit is operable to decode and execute an instruction received from the instruction path and wherein in response to decoding a single instruction specifying an elemental width of operands and a floating-point arithmetic operation, the multi-precision execution unit

(i) partitions data received from the data path and stored in an operand register according to the elemental width specified by the instruction into a plurality of operands stored in partitioned fields of the operand register,

(ii) performs the floating-point arithmetic operation on each of the plurality of operands to produce a plurality of individual results, and

(iii) returns the plurality of individual results to a register as a catenated result, wherein each of the plurality of operands and each of the plurality of individual results comprise floating-point data having a sign bit, an exponent, and a mantissa.

33. (Previously Presented) The data processing system of claim 32, wherein the operand register has a width of 2^n bits, the elemental width is 2^m bits, n and m are each positive integers, and n is greater than m.

34. (Previously Presented) The data processing system of claim 1, wherein the execution unit is capable of decoding and executing a plurality of different data handling instructions, each of the data handling instructions specifying a data handling operation to be applied individually and separately to each of a plurality of operands stored in partitioned fields of an operand register to return a catenated result to a register, where each of the plurality of operands operated on by the data handling operation comprises integer data and the catenated result returned by the data handling operation comprises a plurality of partitioned fields storing the integer data.

35. (Previously Presented) A data processing system, comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to the bus;

(c) a programmable processor coupled to the bus, the programmable processor comprising:

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path; and

an execution unit, coupled to the instruction path and data path, operable to decode and execute instructions received from the instruction path wherein, in response to decoding a single instruction specifying an elemental width of operands and a floating-point arithmetic operation, the execution unit

(i) partitions data received from the data path and stored in an operand register based on the elemental width specified in the instruction into a plurality of operands stored in partitioned fields of the operand register,

(ii) performs the floating-point arithmetic operation on each of the plurality of operands to produce a plurality of individual results, and

(iii) returns the plurality of individual results to a register as a catenated result, where each of the plurality of operands operated on by the floating-point arithmetic operation and each of the plurality of individual results retured by the floating-point arithmetic operation comprise floating-point data having a sign bit, an exponent, and a mantissa, and wherein

the execution unit is capable of decoding and executing a plurality of different data handling instructions, each data handling instruction specifying a data handling operation to be applied individually and separately to each of a plurality of operands stored in partitioned fields of an operand register to return a catenated result to a register, where each of the plurality of operands operated on by the data handling operation

comprises integer data and the catenated result returned by the data handling operation comprises a plurality of partitioned fields storing integer data.

36. (Previously Presented) The data processing system of claim 35, wherein the operand register has a width of 2^n bits, the elemental width is 2^m bits, n and m are each positive integers, and n is greater than m.

37. (Previously Presented) The data processing system of claim 35, wherein the execution unit is capable of performing group floating-point arithmetic operations on floating-point data of at least two different elemental widths.

38. (Previously Presented) The data processing system of claim 35, wherein, in response to decoding a single data handling instruction specifying both a shift amount and a register that has a width of n bits and includes a first plurality of data elements each having an elemental width of m bits that is smaller than the register width with n/m being a positive even integer, the execution unit is further operable to:

(i) shift a most significant subfield of each of the first plurality of data elements by the shift amount towards a least significant bit to produce a second plurality of data elements; and

(ii) provide the second plurality of data elements to partitioned fields of a register in the plurality of registers as a catenated result.

39. (Previously Presented) The data processing system of claim 38, wherein each data element in the first plurality of data elements has a sign bit in a most significant bit position and wherein the execution unit is further operable to fill a shift amount number of most significant

bits in each of the first plurality of data elements with the corresponding sign bit to produce the second plurality of data elements.

40. (Previously Presented) The data processing system of claim 38, wherein the execution unit is further operable to fill a shift amount number of most significant bits in each of the first plurality of data elements with zeros to produce the second plurality of data elements.

41. (Previously Presented) The data processing system of claim 35, wherein one of the plurality of group floating-point arithmetic instructions is for a group square root operation that performs a square root computation on each of the plurality of operands.

42. (Previously Presented) A data processing system comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to the bus;

(c) a programmable microprocessor, coupled to the bus, capable of operation independent of another host processor, the programmable microprocessor comprising:

a virtual memory addressing unit,

an instruction path and a data path,

an external interface operable to receive data from an external source and communicate the received data over the data path,

a cache operable to retain data communicated between the external interface and the data path,

at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path, and

an execution unit, coupled to the instruction path and data path, operable to decode and execute instructions received from the instruction path, wherein the execution unit is configurable to partition data, on an instruction-by-instruction basis, stored in an operand register having a width of n bits into a plurality of operands, each operand having an elemental width of m contiguous bits such that m times the number of operands equals n, the execution unit being capable of executing group floating-point arithmetic instructions that perform a floating-point arithmetic operation on each of the plurality of operands to produce a plurality of individual m-bit results that are returned to a register in the register file as a catenated result, wherein the elemental width of the partitioned data is determined by the instruction and wherein the floating-point data comprises a sign bit, an exponent, and a mantissa.

43. (Previously Presented) The data processing system of claim 42, wherein different group floating-point arithmetic instructions operate on floating-point data of different elemental widths.

44. (Previously Presented) The data processing system of claim 43, wherein a first group floating-point add instruction can specify that the elemental width (m-bits) is one half the width (n-bits) of the operand register and a second group floating-point add instruction can specify that the elemental width (m-bits) is one quarter the width (n-bits) of the operand register.

45. (Previously Presented) The data processing system of claim 42, wherein the execution unit is operable, in response to decoding a single group floating-point add instruction specifying (i) a precision of a group operation corresponding to an elemental width of m-bits of operands, (ii) first and second registers in the register file each having a width of n-bits, partition

each of the first and second registers into n/m floating-point operands, to add the n/m operands stored in partitioned fields of the first register with the n/m operands stored in partitioned fields of the second register to produce n/m floating-point results that are returned to partitioned fields of a register in the plurality of registers as a catenated result.

46. (Previously Presented) The data processing system of claim 42, wherein the execution unit is capable of executing a plurality of different group integer arithmetic instructions, each instruction performing an integer arithmetic operation on each of the plurality of operands to produce a plurality of individual m-bit results that are returned to a register in the register file as a catenated result, wherein the elemental width of the partitioned data is specified in the instruction and wherein different group integer arithmetic instructions operate on integer data of different elemental widths.

47. (Previously Presented) The data processing system of claim 34, 35, or 46 wherein the execution unit comprises a plurality of functional units.

48. (Cancelled).